1-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation and 3-State Outputs

1 FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the Grade 1**
- **Control Input Threshold Referenced to V_{CCA} Voltage**
- **Power-Supply Range: V_{CCA} and V_{CCB}: 1.65V to 5.5V**
- **V_{CC} Isolation: If Either V_{CC} is at GND, Both Ports are in the High-Impedance State**
- **Low Power Consumption, 4μA Max**
- **Output Drive Up to ±24mA@3.0V**
- **No Power-Supply Sequencing Required: Either V_{CCA} or V_{CCB} can be Ramped First**
- **I_{OFF}: Supports Partial-Power-Down Mode Operation**
- **Extended Temperature: -40°C to +125°C**

2 APPLICATIONS

- **ADAS Fusion**
- **ADAS Front Camera**
- **HEV Battery Management System**

3 DESCRIPTIONS

The RS1T45-Q1 is 1-bit non-inverting bus transceiver uses two separate configurable power supply rails. The A port and DIR are designed to track V_{CCA}, which supporting operating voltages from 1.65V to 5.5V, and the B port supporting operating voltages from 1.65V to 5.5V while it tracks the V_{CCB} supply. This allows for universal low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V and 5V voltage nodes.

The RS1T45-Q1 is designed for asynchronous communication between two data buses. The logic levels of the direction- control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry is always active on both A and B ports and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

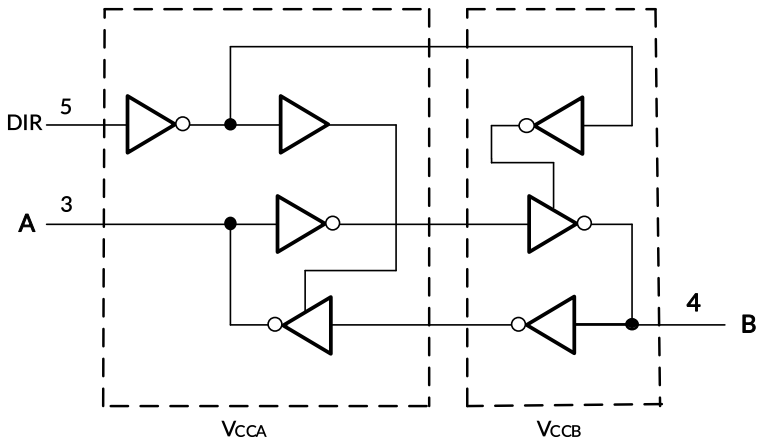
The RS1T45-Q1 is available in Green SOT23-6 and SC70-6 packages. It operates over an ambient temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1T45-Q1	SOT23-6	2.92mm×1.60mm
	SC70-6	2.10mm×1.25mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 FUNCTIONAL BLOCK DIAGRAM



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5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2023/02/27	Initial version completed
A.1.1	2024/03/06	Modify packaging naming
A.2	2024/07/01	1. Update MSL note on Page 4@RevA.1.1 2. Update PACKAGE note

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	PACKAGE LEAD	TEMPERATURE RANGE	Lead finish/Ball material (2)	MSL Peak Temp (3)	PACKAGE MARKING (4)	PACKAGE OPTION
RS1T45 -Q1	RS1T45XC6 -Q1	SC70-6 (5)	-40°C ~+125°C	NIPDAUAG	MSL1-260°-Unlimited	1T45	Tape and Reel, 3000
	RS1T45XH6 -Q1	SOT23-6	-40°C ~+125°C	NIPDAUAG	MSL1-260°-Unlimited	1T45	Tape and Reel, 3000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

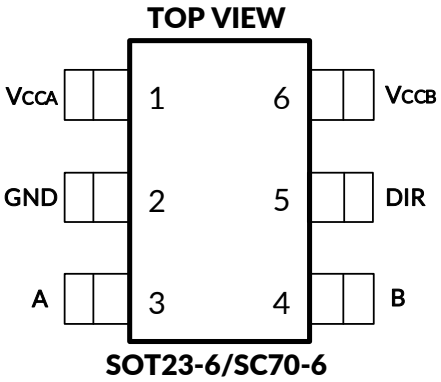
(2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

(4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(5) Equivalent to SOT363.

7 PIN CONFIGURATIONS



7.1 Pin Description

PIN	NAME	TYPE (1)	FUNCTION
SOT23-6/SC70-6			
1	V_{CCA}	P	A Port Supply Voltage. 1.65V ≤ V_{CCA} ≤ 5.5V
2	GND	–	Ground.
3	A	I/O	Input/output A. Reference to V_{CCA}.
4	B	I/O	Input/output B. Reference to V_{CCB}.
5	DIR	I	Direction control. Referenced to V_{CCA}.
6	V_{CCB}	P	B Port Supply Voltage. 1.65V ≤ V_{CCB} ≤ 5.5V.

(1) I=input, O=output, I/O=input and output, P=power.

7.2 Function Table (2)

CONTROL INPUTS (1)	OUTPUT CIRCUITS		OPERATION
DIR	A PORT	B PORT	
L	Enabled	Hi-Z	B data to A bus
H	Hi-Z	Enabled	A data to B bus

Note:
(1) The input circuit of the data I/O is always active.
(2) When either V_{CCA} or V_{CCB} is at GND level, the device goes into suspend mode.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CCA} (3)	Supply Voltage Range		-0.5	6.5	V
V_{CCB} (3)	Supply Voltage Range		-0.5	6.5	V
V_I (2)	Input Voltage Range	A port	-0.5	6.5	V
		B port	-0.5	6.5	
V_O (2)	Voltage range applied to any output in the high-impedance or power-off state	A port	-0.5	V_{CCA}+0.5	V
		B port	-0.5	V_{CCB}+0.5	
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	Vo<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB} or GND			±100	mA
θ_{JA}	Package thermal impedance (4)	SOT23-6		230	°C/W
		SC70-6		265	
T_J	Junction Temperature (5)		-40	150	°C
T_{stg}	Storage temperature		-65	+150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD-51.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-Device Model (CDM), per AEC Q100-011	±500	
		Latch-Up (LU), per AEC Q100-004	±100	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

PARAMETER		V_{CCI} (1)	V_{CCO} (2)	MIN	TYP	MAX	UNIT
Supply Voltage (1)	V_{CCA}			1.65		5.5	V
	V_{CCB}			1.65		5.5	
High-Level Input Voltage (V_{IH})	Data Inputs (4)	1.65V to 1.95V		V_{CCI} x 0.75			V
		2.3V to 2.7V		V_{CCI} x 0.7			
		3V to 3.6V		V_{CCI} x 0.7			
		4.5V to 5.5V		V_{CCI} x 0.7			
Low-Level Input Voltage (V_{IL})	Data Inputs (4)	1.65V to 1.95V				V_{CCI} x 0.35	V
		2.3V to 2.7V				V_{CCI} x 0.3	
		3V to 3.6V				V_{CCI} x 0.3	
		4.5V to 5.5V				V_{CCI} x 0.3	
High-Level Input Voltage (V_{IH})	DIR (referenced to V_{CCA}) (5)	1.65V to 1.95V		V_{CCA} x 0.75			V
		2.3V to 2.7V		V_{CCA} x 0.7			
		3V to 3.6V		V_{CCA} x 0.7			
		4.5V to 5.5V		V_{CCA} x 0.7			
Low-Level Input Voltage (V_{IL})	DIR (referenced to V_{CCA}) (5)	1.65V to 1.95V				V_{CCA} x 0.35	V
		2.3V to 2.7V				V_{CCA} x 0.3	
		3V to 3.6V				V_{CCA} x 0.3	
		4.5V to 5.5V				V_{CCA} x 0.3	
Input Voltage	V_I			0		5.5	V
Output Voltage	V_O			0		V_{CCO}	V
High-Level Output Current (I_{OH})			1.65V to 1.95V			-4	mA
			2.3V to 2.7V			-8	
			3V to 3.6V			-24	
			4.5V to 5.5V			-32	
Low-Level Output Current (I_{OL})			1.65V to 1.95V			4	mA
			2.3V to 2.7V			8	
			3V to 3.6V			24	
			4.5V to 5.5V			32	
Input Transition Rise or Fall Rate($\Delta t/\Delta v$)	Data Inputs (3)	1.65V to 1.95V				20	ns/V
		2.3V to 2.7V				20	
		3V to 3.6V				10	
		4.5V to 5.5V				5	
	Control Inputs	1.65 V to 5.5 V				5	
T_A Operating Free-Air Temperature				-40		125	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power.
(4) For V_{CCI} values not specified in the data sheet, VIH min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(5) For V_{CCA} values not specified in the data sheet, VIH min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

8.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		CONDITIONS	V_{CCA}	V_{CCB}	TEMP	MIN(3)	TYP(4)	MAX(3)	UNIT
V_{OH}		I_{OH} = −100 μA V_I=V_{IH}	1.65V to 4.5V	1.65V to 4.5V	Full	V_{CCO} - 0.1			V
		I_{OH} = −4mA V_I =V_{IH}	1.65V	1.65V		1.2			
		I_{OH} = −8mA V_I =V_{IH}	2.3V	2.3V		1.9			
		I_{OH} = −24mA V_I =V_{IH}	3V	3V		2.4			
		I_{OH} = −32mA V_I =V_{IH}	4.5V	4.5V		3.8			
V_{OL}		I_{OL} = 100 μA V_I =V_{IL}	1.65V to 4.5V	1.65V to 4.5V				0.1	V
		I_{OL} = 4mA V_I =V_{IL}	1.65V	1.65V				0.45	
		I_{OL} = 8mA V_I =V_{IL}	2.3V	2.3V				0.3	
		I_{OL} = 24mA V_I =V_{IL}	3V	3V				0.55	
		I_{OL} = 32mA V_I =V_{IL}	4.5V	4.5V				0.55	
I_I	DIR Input Leakage Current	V_I = V_{CCA} or GND	1.65V to 5.5V	1.65V to 5.5V	+25°C			±1	μA
					Full			±2	
I_{off}	A Port	V_I or V_O= 0 to 5.5V	0V	0V to 5.5V	+25°C			±1	μA
	B Port		0V to 5.5V	0V	Full			±2	
I_{OZ} (5)	A or B Port	V_O=V_{CCO} or GND	1.65V to 5.5V	1.65V to 5.5V	+25°C			±1	μA
					Full			±2	
I_{CCA}	V_{CCA} Supply Current	V_I = V_{CCI} or GND (6) I_O = 0	1.65V to 5.5V	2.3V to 5.5V	Full			3	μA
			5V	0V	Full			2	
			0V	5V	Full			-2	
I_{CCB}	V_{CCB} Supply Current	V_I = V_{CCI} or GND (6) I_O = 0	1.65V to 5.5V	1.65V to 5.5V	Full			3	μA
			5V	0V	Full			-2	
			0V	5V	Full			2	
I_{CCA} + I_{CCB}	Combined Supply Current	V_I = V_{CCI} or GND I_O = 0	1.65V to 5.5V	1.65V to 5.5V	Full			4	μA
ΔI_{CCA}	A port	One A port at V_{CCA} − 0.6 V, DIR at V_{CCA}, B port = open	3V to 5.5V	3V to 5.5V	Full			50	μA
	DIR	DIR at V_{CCA} − 0.6V, B port = open A port at V_{CCA} or GND			Full			50	μA
ΔI_{CCB}	B port	One B port at V_{CCB} − 0.6 V, DIR at GND, A port = open	3V to 5.5V	3V to 5.5V	Full			50	μA
C_I	Input Capacitance	DIR	3.3V	3.3V	+25°C		4		pF
C_{IO}	Input-to-Output Internal Capacitance	A port or B Port	3.3V	3.3V	+25°C		8.5		pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(5) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(6) Hold all unused data inputs of the device at V_{CCI} or GND to assure proper device operation.

8.5 Timing Requirements

8.5.1 V_{CCA}=1.8V± 0.15 V

over recommended operating free-air temperature range, Full=-40°C to 125°C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	V_{CCB}=1.8V ±0.15V (1)		V_{CCB}=2.5V ±0.2V (1)		V_{CCB}=3.3V ±0.3V (1)		V_{CCB}=5V ±0.5V (1)		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	Full	3.5	24.6	2.6	17.2	2.0	18.6	1.6	18.5	ns
t_{PHL}			Full	3.3	18.4	2.6	15.5	2.1	16.4	2.0	16.8	
t_{PLH}	B	A	Full	3.5	24.6	2.7	24.5	2.5	23.2	2.2	23.2	ns
t_{PHL}			Full	3.3	18.4	2.5	18.4	2.4	15.3	2.1	14.1	
t_{PHZ}	DIR	A	Full	6.2	33.9	5.7	37.1	5.6	32.3	6.1	31.9	ns
t_{PLZ}			Full	2.7	35.9	2.5	37.3	2.8	17.8	3.7	41.7	
t_{PHZ}	DIR	B	Full	8.8	33.9	5.8	30.0	4.3	33.2	2.7	34.6	ns
t_{PLZ}			Full	5.0	35.9	2.6	23.6	2.7	22.4	2.4	22.2	
t_{PZH} (2)	DIR	A	Full		60.5		48.1		45.6		45.4	ns
t_{PZL} (2)			Full		52.3		48.4		48.5		48.7	
t_{PZH} (2)	DIR	B	Full		60.5		54.5		36.4		60.2	ns
t_{PZL} (2)			Full		52.3		52.6		48.7		48.7	

(1) This parameter is ensured by design and/or characterization and is not tested in production.
(2) The enable time is a calculated value, derived using the formula shown in Enable Times.

8.5.2 V_{CCA}=2.5V±0.2 V

over recommended operating free-air temperature range, Full=-40°C to 125°C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	V_{CCB}=1.8V ±0.15V (1)		V_{CCB}=2.5V ±0.2V (1)		V_{CCB}=3.3V ±0.3V (1)		V_{CCB}=5V ±0.5V (1)		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	Full	2.7	24.5	1.8	16.5	1.5	15.4	1.3	16.6	ns
t_{PHL}			Full	2.5	18.4	1.6	12.7	1.5	11.3	1.0	10.4	
t_{PLH}	B	A	Full	2.6	17.2	1.8	16.5	1.6	16.2	1.2	16.2	ns
t_{PHL}			Full	2.6	15.5	1.6	12.7	1.5	12.5	1.0	11.4	
t_{PHZ}	DIR	A	Full	3.6	30.0	2.5	32.8	2.7	33.2	3.8	32.4	ns
t_{PLZ}			Full	1.5	23.6	1.5	25.7	1.5	14.8	1.2	18.1	
t_{PHZ}	DIR	B	Full	7.8	37.1	4.9	32.8	3.6	33.2	2.2	34.3	ns
t_{PLZ}			Full	4.2	37.3	2.6	25.7	3.0	26.4	1.9	26.4	
t_{PZH} (2)	DIR	A	Full		54.5		42.2		42.6		42.6	ns
t_{PZL} (2)			Full		52.6		45.5		45.7		45.7	
t_{PZH} (2)	DIR	B	Full		48.1		42.2		30.2		34.7	ns
t_{PZL} (2)			Full		48.4		45.5		44.5		42.8	

(1) This parameter is ensured by design and/or characterization and is not tested in production.
(2) The enable time is a calculated value, derived using the formula shown in Enable Times.

8.5.3 V_{CCA}=3.3V±0.3 V

over recommended operating free-air temperature range, Full=-40°C to 125°C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	V_{CCB}=1.8V ±0.15V (1)		V_{CCB}=2.5V ±0.2V (1)		V_{CCB}=3.3V ±0.3V (1)		V_{CCB}=5V ±0.5V (1)		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	Full	2.5	23.2	1.6	16.2	0.8	15.2	0.8	15.1	ns
t_{PHL}			Full	2.4	15.3	1.5	12.5	0.9	10.2	0.8	10.0	
t_{PLH}	B	A	Full	2.0	18.6	1.5	15.4	0.8	15.2	0.7	15.8	ns
t_{PHL}			Full	2.1	16.4	1.5	11.3	0.9	10.2	0.8	10.4	
t_{PHZ}	DIR	A	Full	2.7	33.2	2.8	33.2	1.8	34.3	2.8	32.8	ns
t_{PLZ}			Full	2.1	22.4	1.9	26.4	2.2	15.1	2.4	19.5	
t_{PHZ}	DIR	B	Full	6.4	32.3	4.6	33.2	3.4	34.3	2.0	34.1	ns
t_{PLZ}			Full	2.7	17.8	2.5	14.8	2.8	15.1	1.8	14.8	
t_{PZH} (2)	DIR	A	Full		36.4		30.2		30.3		30.6	ns
t_{PZL} (2)			Full		48.7		44.5		44.5		44.5	
t_{PZH} (2)	DIR	B	Full		45.6		42.6		30.3		34.6	ns
t_{PZL} (2)			Full		48.5		45.7		44.5		42.8	

(1) This parameter is ensured by design and/or characterization and is not tested in production.
(2) The enable time is a calculated value, derived using the formula shown in Enable Times.

8.5.4 V_{CCA}=5V±0.5 V

over recommended operating free-air temperature range, Full=-40°C to 125°C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	V_{CCB}=1.8V ±0.15V (1)		V_{CCB}=2.5V ±0.2V (1)		V_{CCB}=3.3V ±0.3V (1)		V_{CCB}=5V ±0.5V (1)		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	Full	2.2	23.2	1.2	16.2	0.7	15.8	0.6	15.2	ns
t_{PHL}			Full	2.1	14.1	1.0	11.4	0.8	10.4	0.6	9.5	
t_{PLH}	B	A	Full	1.6	18.5	1.3	16.6	0.8	15.1	0.6	15.2	ns
t_{PHL}			Full	2.0	16.8	1.0	10.4	0.8	10.0	0.6	9.5	
t_{PHZ}	DIR	A	Full	2.5	34.6	2.4	34.3	2.6	34.1	2.4	33.4	ns
t_{PLZ}			Full	1.0	22.2	1.2	26.4	1.2	14.8	1.0	19.0	
t_{PHZ}	DIR	B	Full	5.7	31.9	3.0	32.4	1.2	32.8	2.0	33.4	ns
t_{PLZ}			Full	3.1	41.7	2.4	18.1	3.0	19.5	1.9	19.0	
t_{PZH} (2)	DIR	A	Full		60.2		34.7		34.6		34.2	ns
t_{PZL} (2)			Full		48.7		42.8		42.8		42.9	
t_{PZH} (2)	DIR	B	Full		45.4		42.6		30.6		34.2	ns
t_{PZL} (2)			Full		48.7		45.7		44.5		42.9	

(1) This parameter is ensured by design and/or characterization and is not tested in production.
(2) The enable time is a calculated value, derived using the formula shown in Enable Times.

8.6 Operating Characteristics

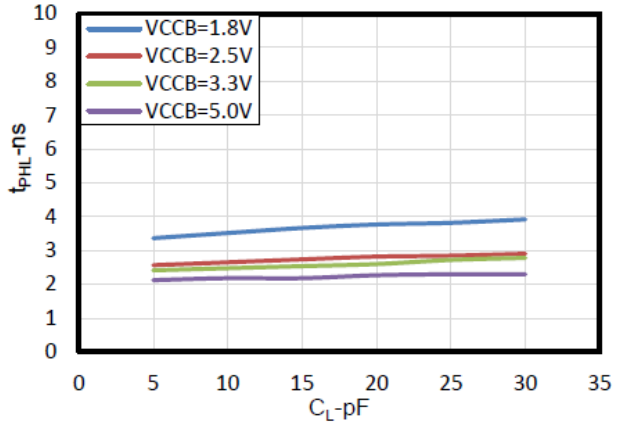
T_A=25°C

PARAMETER		TEST CONDITIONS	V_{CCA}= V_{CCB}=1.8V	V_{CCA}= V_{CCB}=2.5V	V_{CCA}= V_{CCB}=3.3V	V_{CCA}= V_{CCB}=5V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA}(1)	A-port input, B-port output	C_L=0, f=10MHz, t_r=t_f=5ns	3	4	6	9	pF
	B-port input, A-port output		14	17	22	32	
C_{pdB}(1)	A-port input, B-port output		14	16	21	32	
	B-port input, A-port output		3	4	6	9	

(1) Power dissipation capacitance per transceiver.

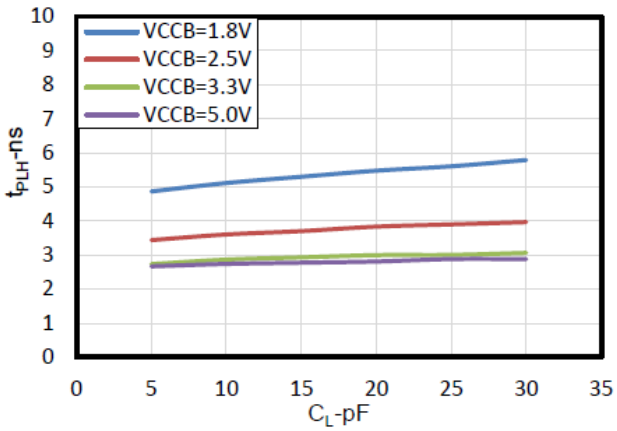
8.7 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.



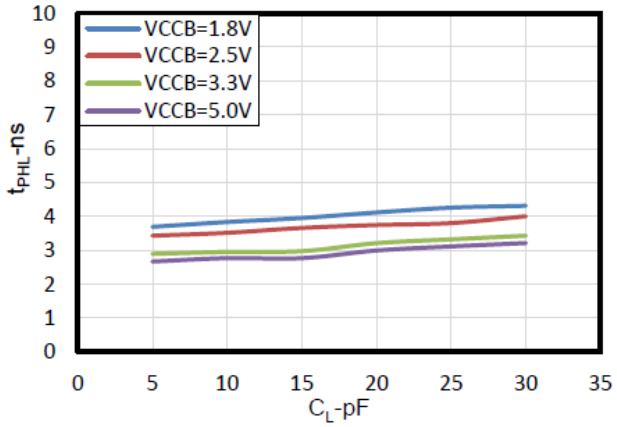
T_A = 25°C, V_{CCA} = 1.8 V

Figure 1. Typical Propagation Delay High-to-Low (A to B) vs Load Capacitance



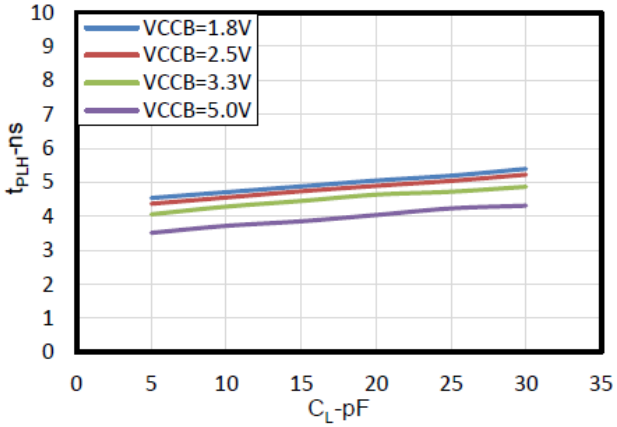
T_A = 25°C, V_{CCA} = 1.8 V

Figure 2. Typical Propagation Delay Low-to-High (B to A) vs Load Capacitance



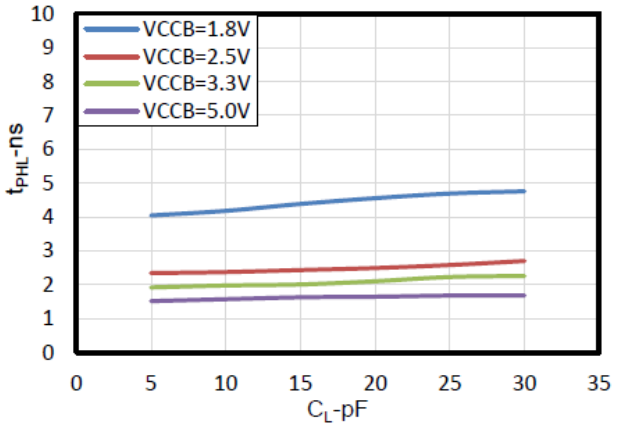
T_A = 25°C, V_{CCA} = 2.5 V

Figure 3. Typical Propagation Delay High-to-Low (A to B) vs Load Capacitance



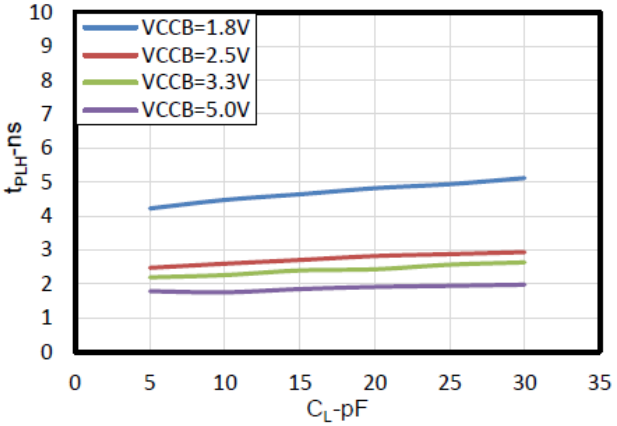
T_A = 25°C, V_{CCA} = 2.5 V

Figure 4. Typical Propagation Delay Low-to-High (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 3.3 V

Figure 5. Typical Propagation Delay High-to-Low (A to B) vs Load Capacitance

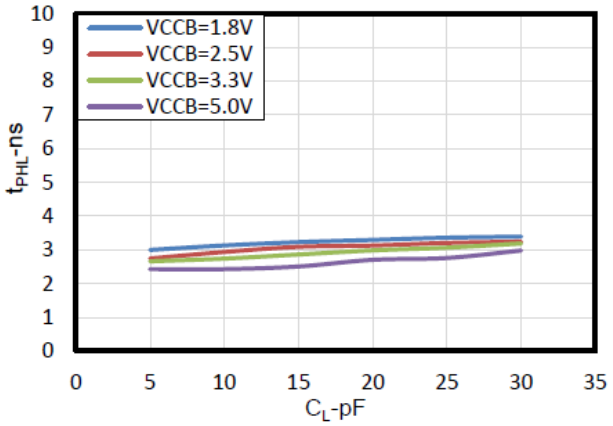


T_A = 25°C, V_{CCA} = 3.3 V

Figure 6. Typical Propagation Delay Low-to-High (B to A) vs Load Capacitance

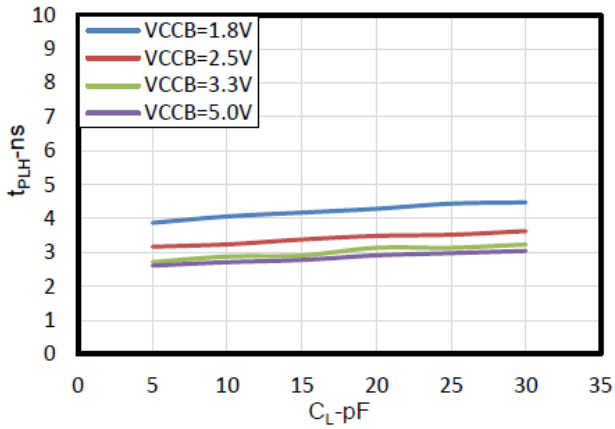
Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.



T_A = 25°C, V_{CCA} = 5 V

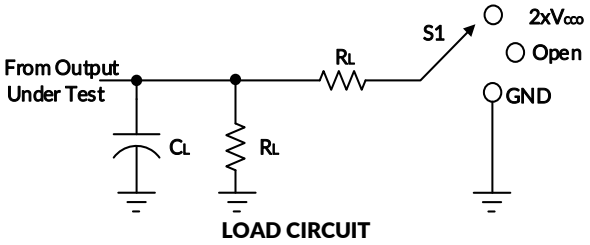
Figure 7. Typical Propagation Delay High-to-Low (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 5 V

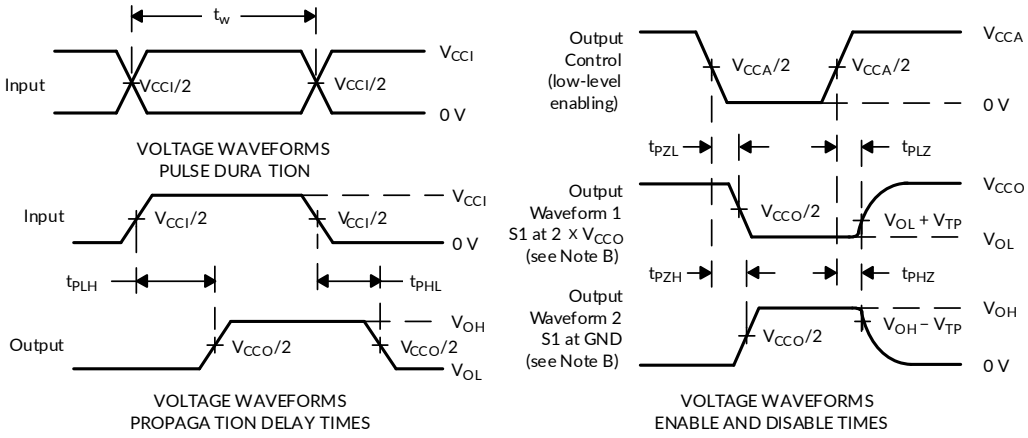
Figure 8. Typical Propagation Delay Low-to-High (B to A) vs Load Capacitance

9 PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 X V_{CCO}
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{TP}
1.8V±0.15V	15pF	2kΩ	0.15V
2.5V±0.2V	15pF	2kΩ	0.15V
3.3V±0.3V	15pF	2kΩ	0.3V
5V±0.5V	15pF	2kΩ	0.3V



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, Z_O = 50 Ω, dv/dt≥1V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. All parameters and waveforms are not applicable to all devices.

Figure 9. Load Circuit and Voltage Waveforms

10 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The RS1T45-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum output current can be up to 32 mA when device is powered by 5 V.

10.1.1 Enable Times

Calculate the enable times for the RS1T45-Q1 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the RS1T45-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

10.2 Typical Application

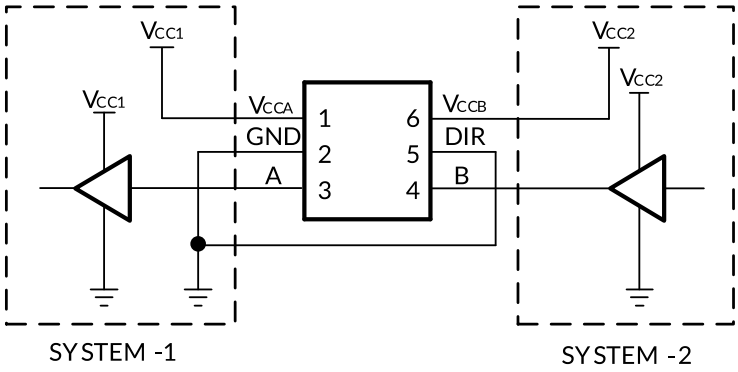


Figure 10. Unidirectional Logic Level-Shifting Application (B to A)

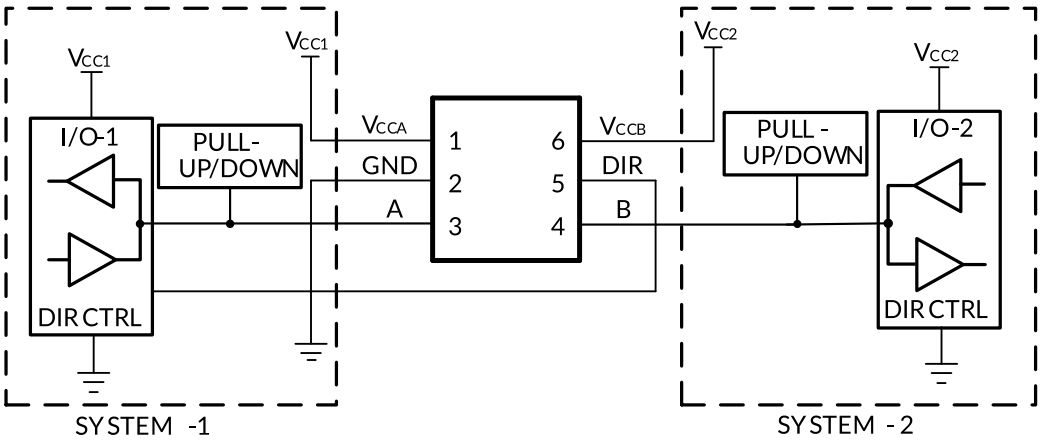


Figure 11. Bidirectional Logic Level-Shifting Application (B to A or A to B)

11 LAYOUT

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

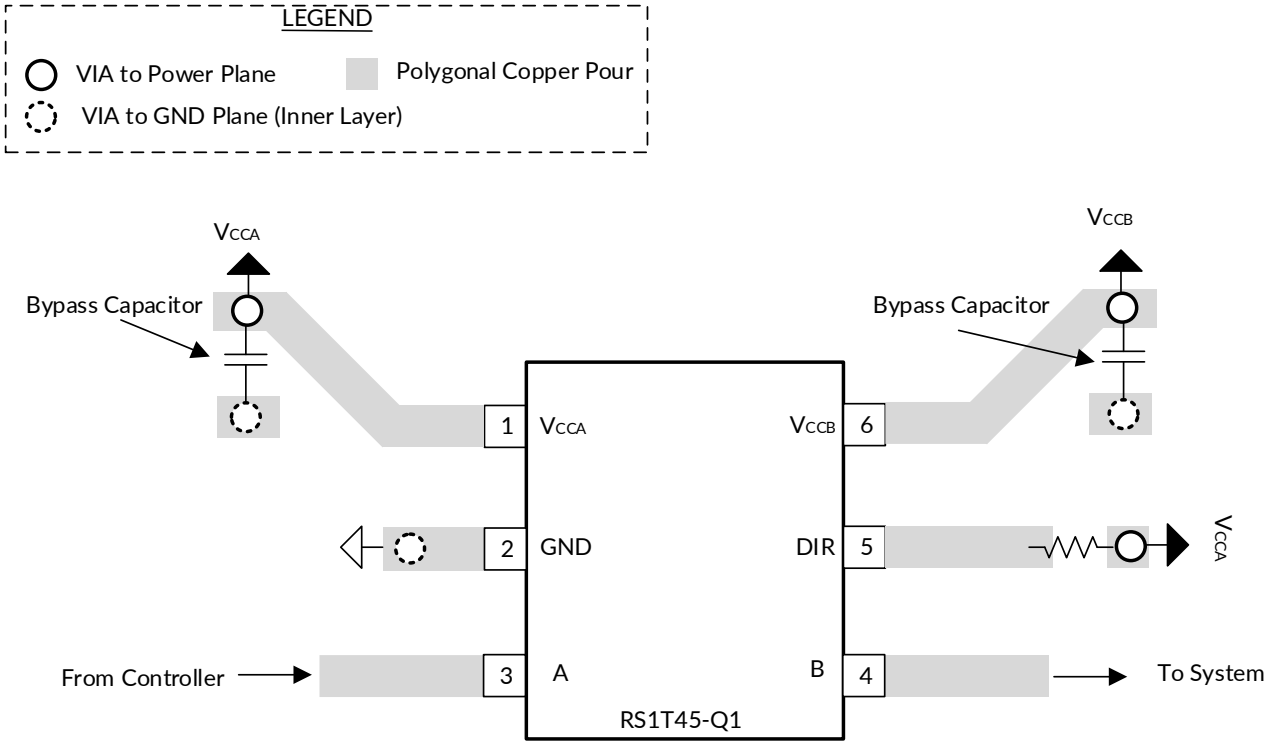
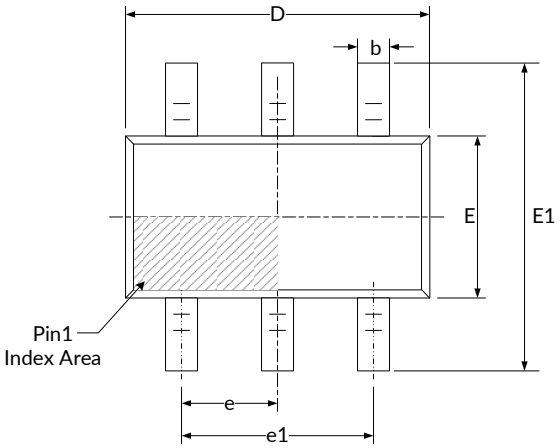
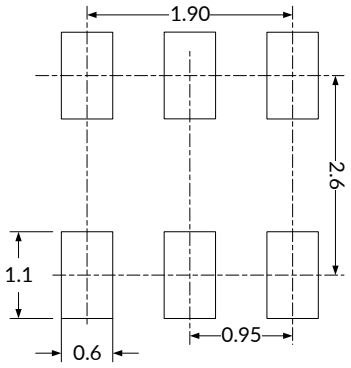


Figure 12. Layout Example

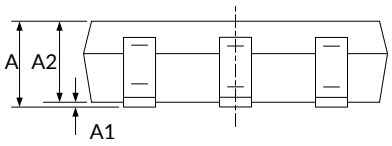
12 PACKAGE OUTLINE DIMENSIONS

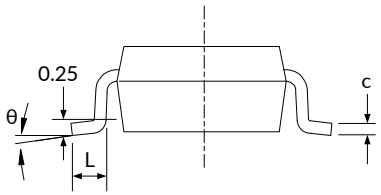
SOT23-6 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



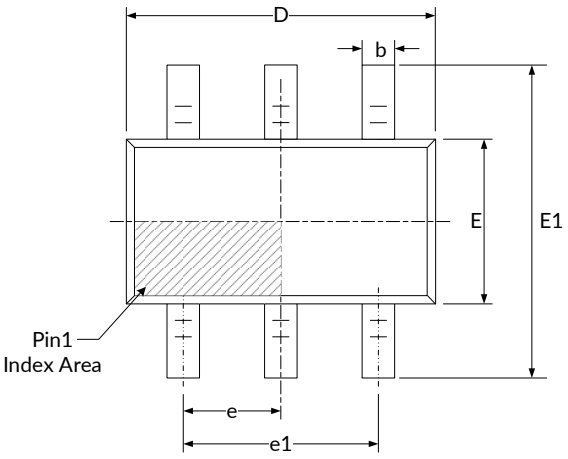


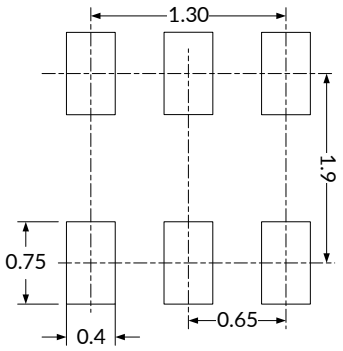
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.250		0.049
A1	0.040	0.100	0.001	0.004
A2	1.000	1.200	0.040	0.047
b	0.330	0.410	0.012	0.016
c	0.150	0.190	0.006	0.007
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC) (2)		0.037 (BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

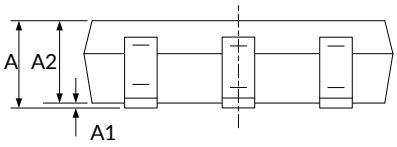
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

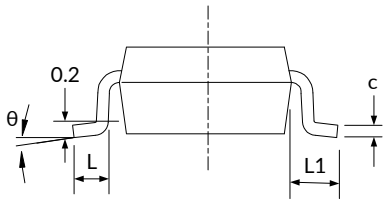
SC70-6 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D (1)	2.000	2.200	0.079	0.087
E (1)	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 (BSC) (2)		0.026 (BSC) (2)	
e1	1.300 (BSC) (2)		0.051 (BSC) (2)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

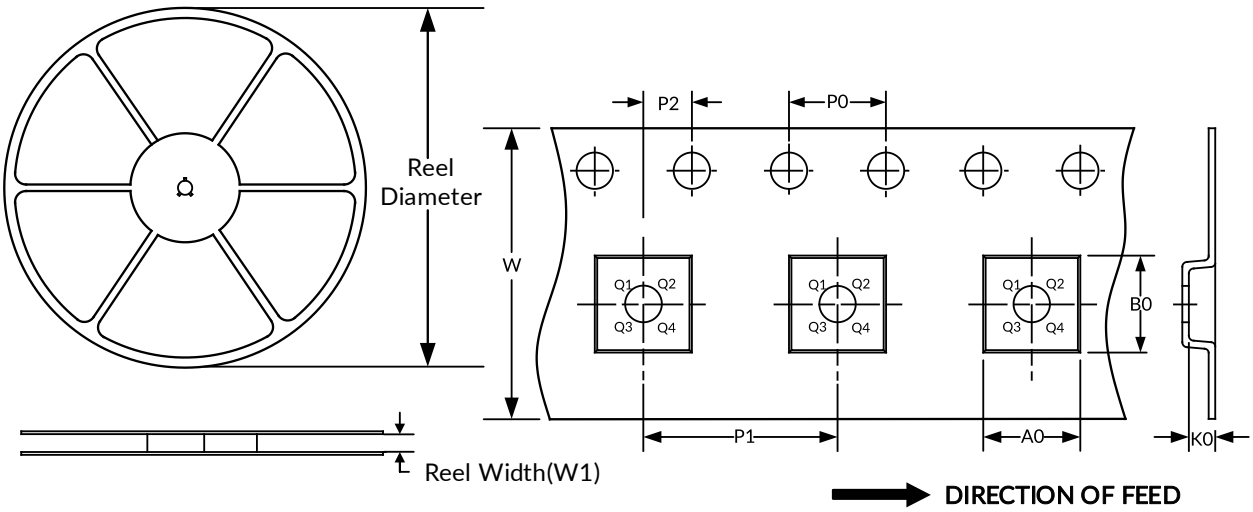
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-6	7”	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3
SC70-6	7”	9.5	2.40	2.50	1.20	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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