RS175 Quadruple D-Type Flip-Flop with Clear

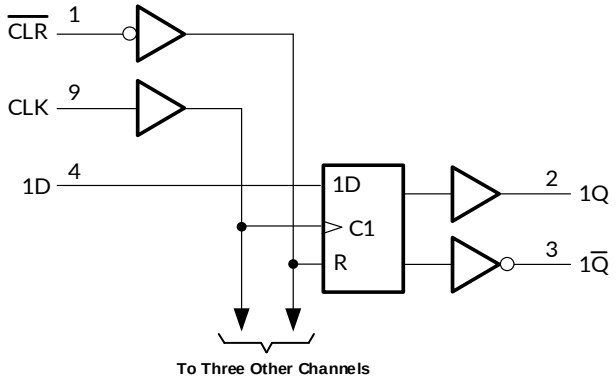
1 FEATURES

- **Operating Voltage Range: 1.65V to 5.5V**
- **Low Power Consumption: 8μA (Max)**
- **Four edge-triggered D-type flip-flops**
- **Asynchronous master reset**
- **Operating Temperature Range: -40°C to +125°C**
- **Micro SIZE PACKAGES: SOP16, TSSOP16**

2 APPLICATIONS

- **Buffer/Storage Registers**
- **Shift Registers**
- **Pattern Generators**

Logic Diagram (Positive Logic)



3 DESCRIPTIONS

The RS175 is a quad positive-edge triggered D-type flip-flop with individual data inputs (nD) and complementary outputs (nQ and n$\overline{Q}$). The common clock (CLK) and master reset ($\overline{CLR}$) inputs load and reset all flip-flops simultaneously. The D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. A LOW on $\overline{CLR}$ causes the flip-flops and outputs to be reset LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

This device available in Green SOP16 and TSSOP16 packages. It operates over an ambient temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS175	SOP16	9.90mm×3.90mm
	TSSOP16	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.1	2023/12/06	Initial version completed
A.1.1	2024/02/29	Modify packaging naming

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS175	RS175XTSS16	-40°C ~+125°C	TSSOP16	RS175	MSL3	Tape and Reel,4000
	RS175XS16	-40°C ~+125°C	SOP16	RS175	MSL3	Tape and Reel,4000

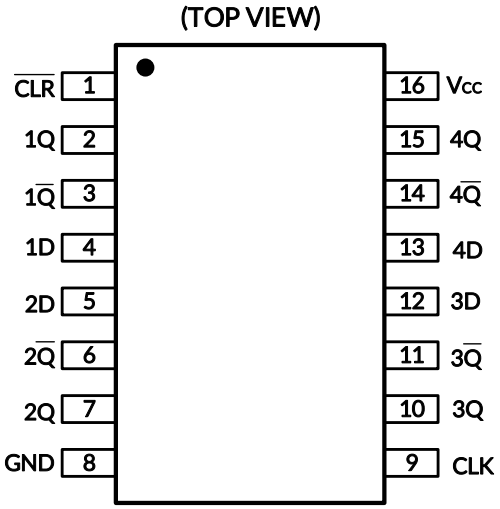
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

6 PIN CONFIGURATIONS



6.1 PIN DESCRIPTION

PIN	NAME	I/O TYPE (1)	FUNCTION
TSSOP16/SOP16			
1	$\overline{CLR}$	I	Clear Data Input
2	1Q	O	Output
3	$1\overline{Q}$	O	Output
4	1D	I	Input
5	2D	I	Input
6	$2\overline{Q}$	O	Output
7	2Q	O	Output
8	GND	P	Ground
9	CLK	I	Clock Input
10	3Q	O	Output
11	$3\overline{Q}$	O	Output
12	3D	I	Input
13	4D	I	Input
14	$4\overline{Q}$	O	Output
15	4Q	O	Output
16	V_{CC}	P	Power pin

(1) I=input, O=output, P=power.

6.2 FUNCTION TABLE

INPUTS			OUTPUT	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

(1) H=High Voltage Level; L=Low Voltage Level; X=Don't Care

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
I_{IK}	Input clamp current	V_I<0 or V_I > V_{CC}		±20	mA
I_{OK}	Output clamp current	V_O<0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance (3)	TSSOP16		45	°C/W
		SOP16		150	
T_J	Junction temperature (4)		-65	150	°C
Tstg	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD-51.

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±2000	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000	
		Machine Model (MM), JESD22-A115	±200	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full=-40°C to 125°C, unless otherwise noted.) (1)

8.1 Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC}	Operating	1.65	5.5	V
High-level input voltage	V_{IH}	V_{CC} = 2 V	1.5		V
		V_{CC} = 3.3 V	2.4		
		V_{CC} =4.5 V	3.15		
		V_{CC} = 5.5 V	3.85		
Low-level input voltage	V_{IL}	V_{CC} = 2 V		0.5	V
		V_{CC} = 3.3 V		1	
		V_{CC} =4.5 V		1.35	
		V_{CC} = 5.5 V		1.65	
Input voltage	V_I		0	V_{CC}	V
Output voltage	V_O		0	V_{CC}	V
Input transition rise or fall	Δt / Δv	V_{CC} = 2 V		1000	ns
		V_{CC} = 3.3 V		600	
		V_{CC} =4.5 V		500	
		V_{CC} = 5.5 V		400	
Operating temperature	T_A		-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

8.2 DC Characteristics

PARAMETER	TEST CONDITIONS	V_{CC}	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OH}	I_{OH} = -20μA	2V	Full	1.9			V
		3.3V		3.2			
		4.5V		4.4			
		5.5V		5.4			
	I_{OH} = -4mA	4.5V		3.84			
	I_{OH} = -5.2mA	5.5V		4.69			
V_{OL}	I_{OL} = 20μA	2V	Full			0.1	V
		3.3V				0.1	
		4.5V				0.1	
		5.5V				0.1	
	I_{OL} = 4mA	4.5V				0.5	
	I_{OL} = 5.2mA	5.5V				0.55	
I_I	V_I=5.5V or GND	5.5V	+25°C		±0.1	±1	μA
			Full			±2	
I_{CC}	V_I=5.5V or GND, I_O=0	5.5V	+25°C			8	μA
			Full			80	
C_i (Input Capacitance)		1.65 V to 5.5 V	+25°C		4	10	pF
			Full			10	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

8.3 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (1)

		V_{CC}	T_A = 25°C			T_A=-40°Cto 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{clock} Clock frequency		2			6		5	MHz
		3.3			18		15	
		4.5			31		25	
		5.5			33		27	
t_w Pulse duration	$\overline{CLR}$ low	2	40			52		ns
		3.3	20			30		
		4.5	8			10		
		5.5	6			8		
	CLK High or low	2	40			52		
		3.3	20			30		
		4.5	8			10		
		5.5	6			8		
t_{su} Setup time before CLK ↑	Data	2	50			65		ns
		3.3	30			38		
		4.5	10			12		
		5.5	8			10		
	$\overline{CLR}$ inactive	2	50			65		
		3.3	30			38		
		4.5	10			12		
		5.5	8			10		
t_h Hold time, data after CLK ↑		2		6.1				ns
		3.3		2.6				
		4.5		2				
		5.5		1.8				

(1) This parameter is ensured by design and/or characterization and is not tested in production.

8.4 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A=-40°Cto 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			2	6	12		5		MHz
			3.3	18	30		15		
			4.5	31	50		25		
			5.5	33	55		27		
t_{pd}	$\overline{CLR}$	Any	2		17	25.5		28.5	ns
			3.3		8	12		13.5	
			4.5		6	9		10	
			5.5		5.5	8.5		9.5	
	CLK	Any	2		23.5	35		39	
			3.3		10.5	16		18	
			4.5		8.5	13		13.5	
			5.5		7.5	11.5		12	
t_t		Any	2		10.5	15.5		18	ns
			3.3		5.5	8.5		10	
			4.5		4.5	7		8.5	
			5.5		4	6		7.5	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

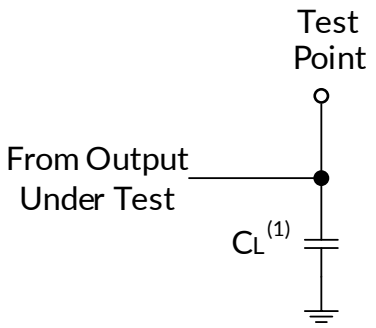
8.5 Operating Characteristics

T_A = +25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per flip-flop	No load	35	pF

9 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.
For clock inputs, f_{max} is measured when the input duty cycle is 50%.
The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 1. Load Circuit for Push-Pull Outputs

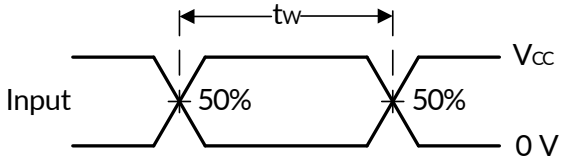


Figure 2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

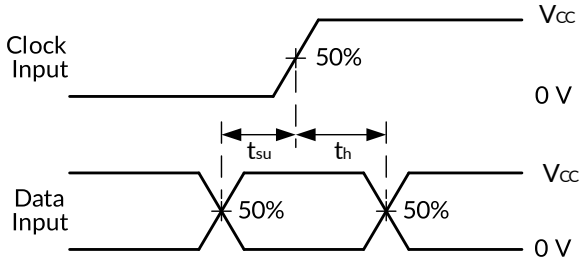
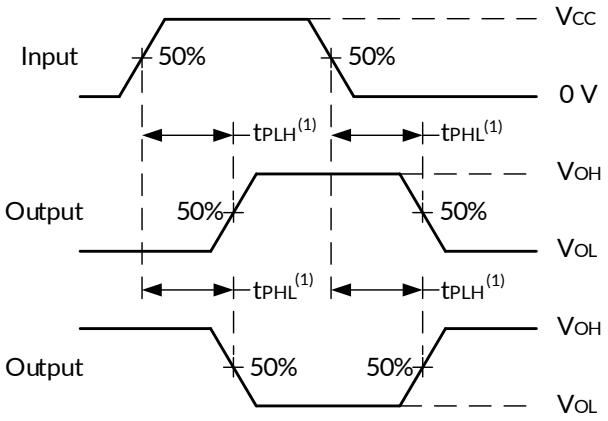
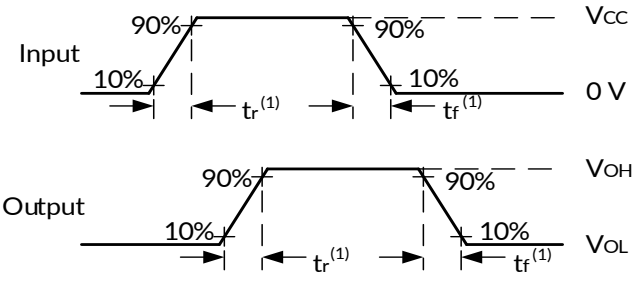


Figure 3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t.

Figure 5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

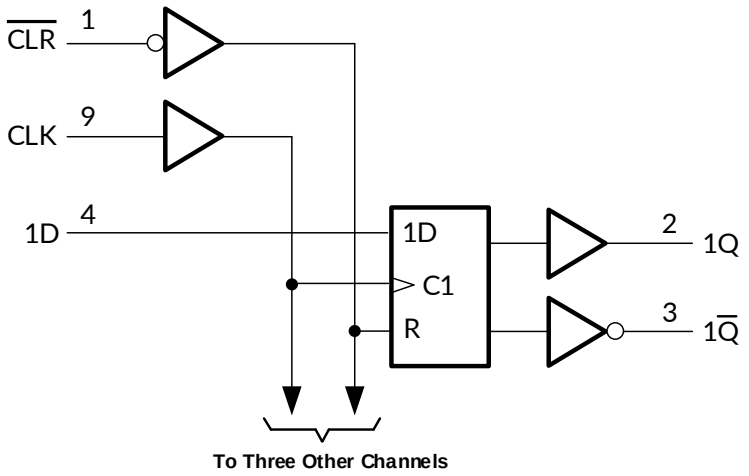
10 Detailed Description

10.1 Overview

These positive-edge-triggered D-type flip-flops have a direct clear ($\overline{CLR}$) input. The RS175 devices feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

10.2 Functional Block Diagram



11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

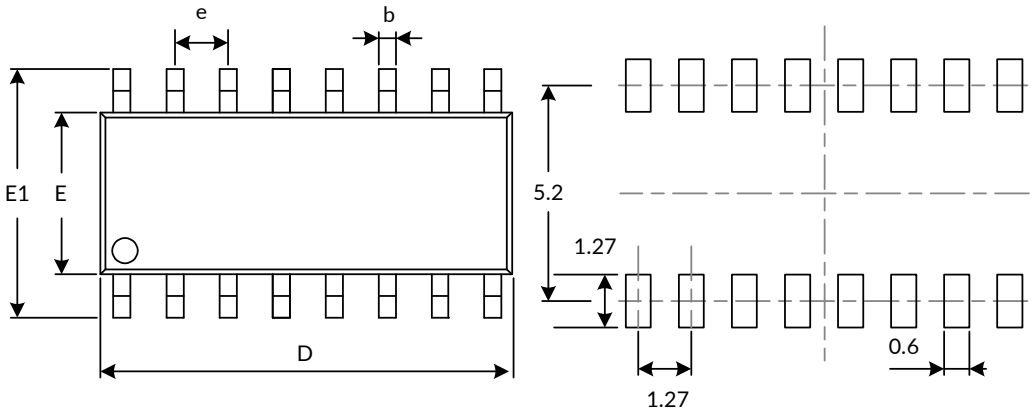
12 Layout

12.1 Layout Guidelines

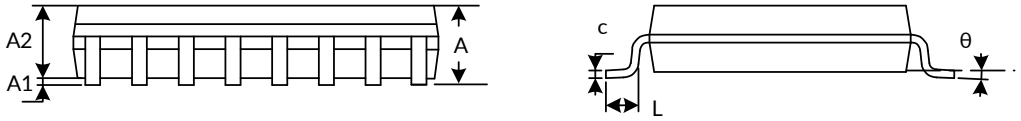
When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

13 PACKAGE OUTLINE DIMENSIONS

SOP16 (3)



RECOMMENDED LAND PATTERN (Unit: mm)

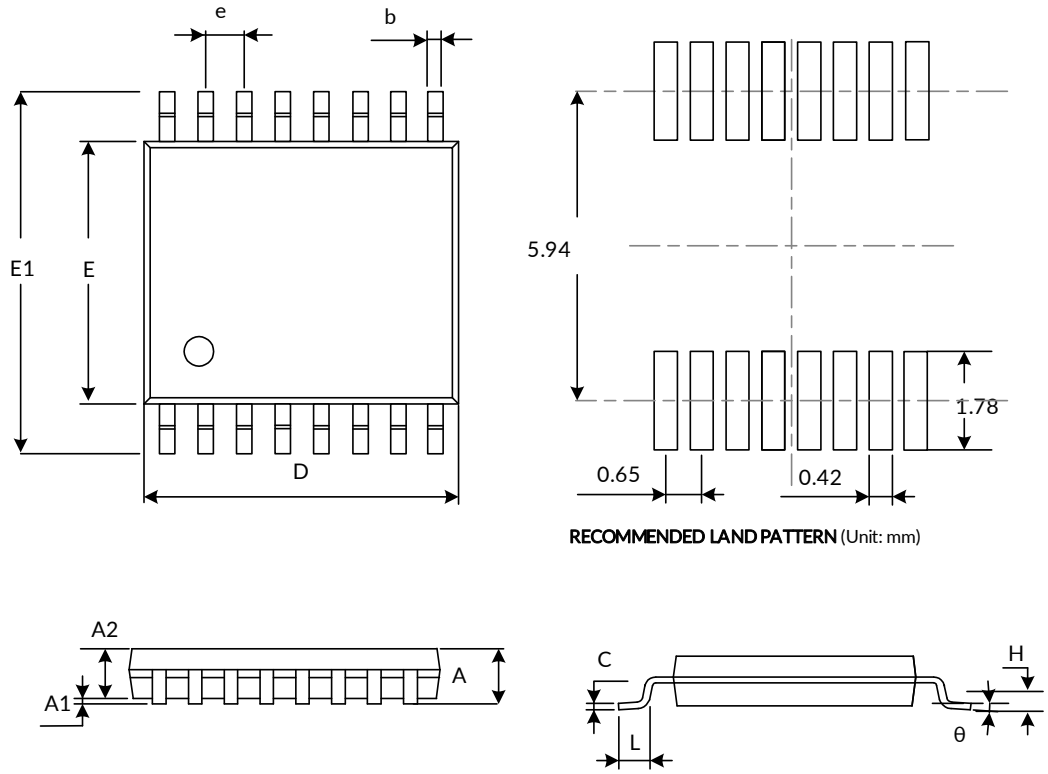


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D (1)	9.800	10.200	0.386	0.402
E (1)	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27(BSC) (2)		0.050(BSC) (2)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

TSSOP16 (3)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D (1)	4.860	5.100	0.191	0.201
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.500	0.700	0.02	0.028
H	0.25TYP		0.01TYP	
θ	1°	7°	1°	7°

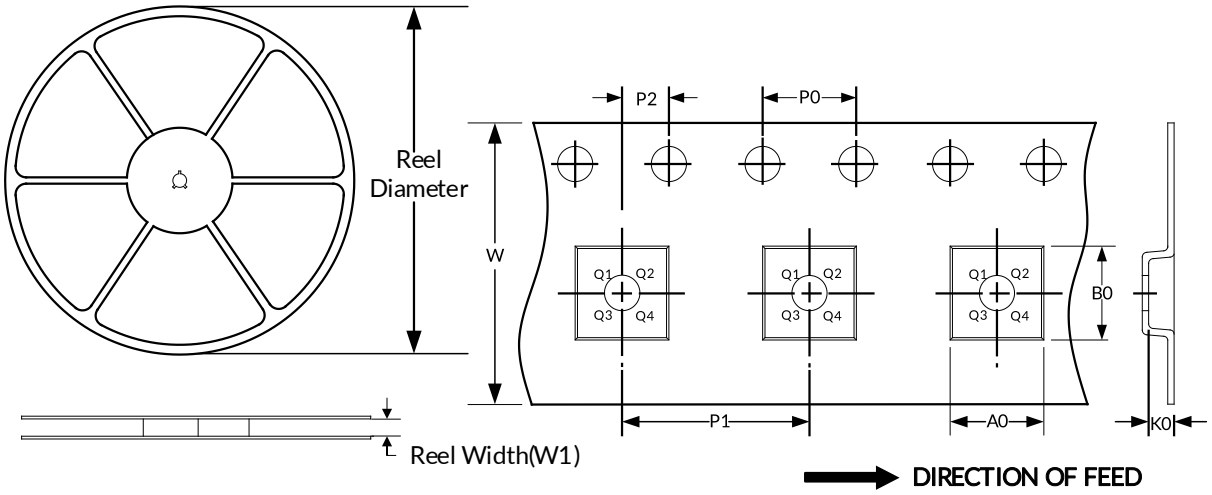
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOP16	13”	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP16	13”	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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