RS1G373-Q1 Single D-Type Latch With 3-State Output

1 FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the Grade 1**
- **Operating Voltage Range:1.65V to 5.5V**
- **Low Power Consumption:10μA (Max)**
- **Operating Temperature Range: -40°C to +125°C**
- **Inputs Accept Voltage to 5.5V**
- **High Output Drive: ±24mA at V_{CC}=3.0V**
- **I_{off} Supports Live Insertion, Partial-Power Down Mode, and Back-Drive Protection**
- **Micro SIZE PACKAGES: SC70-6**

2 APPLICATIONS

- **HEV/EV Battery Management System (BMS)**
- **Automotive Infotainment & Cluster**
- **Automotive HEV/EV Powertrain**

3 DESCRIPTIONS

The RS1G373-Q1 device is a single D-type latch is designed for 1.65V to 5.5V V_{CC} operation.

This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers and working registers. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

$\overline{OE}$ does not affect the internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The RS1G373-Q1 is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

This device available in Green SC70-6 packages. It operates over an ambient temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1G373-Q1	SC70-6	2.10mm×1.25mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.1	2024/05/20	Initial version completed

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	Lead finish/Ball material (2)	MSL Peak Temp (3)	PACKAGE MARKING (4)	PACKAGE OPTION
RS1G373-Q1	RS1G373XC6-Q1	-40°C ~+125°C	SC70-6 (5)	NIPDAUAG	MSL1-260°-Unlimited	1G373	Tape and Reel,3000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

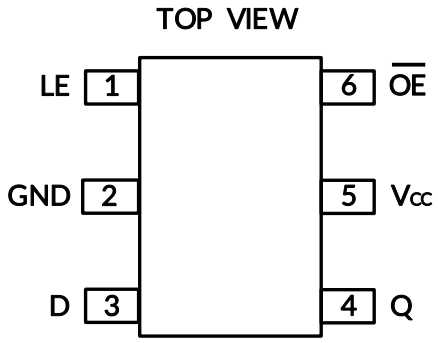
(2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(3) MSL Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(5) Equivalent to SOT363.

6 PIN CONFIGURATIONS



SC70-6

6.1 PIN DESCRIPTION

PIN	NAME	I/O TYPE (1)	FUNCTION
SC70-6			
1	LE	I	Latch Enable; output follows D input when high
2	GND	-	Ground
3	D	I	D latch input
4	Q	O	Q latch output
5	V_{CC}	-	Supply Voltage
6	$\overline{OE}$	I	Active low output enable; Hi-Z output when high

(1) I=input, O=output, P=power.

6.2 FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	L	L
L	H	H	H
L	L	X	Q_0
H	X	X	Hi-Z

(1) H=High Voltage Level
L=Low Voltage Level
X=Don't Care

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power-off state (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state (2) (3)		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance (4)	SC70-6		265	°C/W
T_J	Junction temperature (5)		-65	150	°C
Tstg	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-Device Model (CDM), per AEC Q100-011	±1000	
		Latch-Up (LU), per AEC Q100-004	±150	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full=-40°C to 125°C, unless otherwise noted.) (1)

8.1 Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC}	Operating	1.65	5.5	V
High-level input voltage	V_{IH}	V_{CC}=1.65V to 1.95V	0.75 × V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2.3		
		V_{CC}=4.5V to 5.5V	0.7 × V_{CC}		
Low-level input voltage	V_{IL}	V_{CC}=1.65V to 1.95V		0.25 × V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3 × V_{CC}	
Input voltage	V_I		0	5.5	V
Output voltage	V_O		0	V_{CC}	V
High-level output current	I_{OH}	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
Low-level output current	I_{OL}	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Input transition rise or fall	Δt / Δv	V_{CC}=1.8V± 0.15V,2.5V ± 0.2V		20	ns/V
		V_{CC}=3.3V± 0.3V		10	
		V_{CC}=5V± 0.5V		5	
Operating temperature	T_A		-40	125	℃

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

8.2 DC Characteristics

PARAMETER		TEST CONDITIONS	V_{CC}	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OH}		I_{OH} = -100μA	1.65V to 5.5V	Full	V_{CC}-0.1			V
		I_{OH} = -4mA	1.65V		1.2			
		I_{OH} = -8mA	2.3V		1.9			
		I_{OH} = -16mA	3V		2.4			
		I_{OH} = -24mA			2.3			
		I_{OH} = -32mA	4.5V		3.8			
V_{OL}		I_{OL} = 100μA	1.65V to 5.5V	Full			0.1	V
		I_{OL} = 4mA	1.65V				0.45	
		I_{OL} = 8mA	2.3V				0.3	
		I_{OL} = 16mA	3V				0.4	
		I_{OL} = 24mA					0.55	
		I_{OL} = 32mA	4.5V				0.55	
I_I	Data or control inputs	V_I=5.5V or GND	0V to 5.5V	+25°C		±0.1	±1	μA
				Full			±5	
I_{OZ}		V_O=0V to 5.5V	3.6V	+25°C		±0.1	±1	μA
				Full			±5	
I_{off}		V_I or V_O=5.5V	0	+25°C		±0.1	±1	μA
				Full			±10	
I_{CC}		V_I=5.5V or GND, I_O=0	1.65V to 5.5V	+25°C		0.1	1	μA
				Full			10	
ΔI_{CC}		One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND	3V to 5.5V	Full			500	μA
C_i (Input Capacitance)		V_I = V_{CC} or GND	3.3V	+25°C		4		pF
C_O (Output Capacitance)		V_O= V_{CC} or GND	3.3V	+25°C		6		pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

8.3 Timing Requirements

over recommended operating free-air temperature range (T_A = +25°C, unless otherwise noted) (1)

PARAMETER		V_{CC}=1.8V±0.15 V		V_{CC}=2.5V±0.2 V		V_{CC}=3.3V±0.3 V		V_{CC}=5V±0.5 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	11		5.5		3.5		2.5		ns
t_{su}	Setup time, data before LE↓	8		3.5		2		1.5		
t_h	Hold time, data after LE↓	2		1.5		1.5		1.5		

(1) This parameter is ensured by design and/or characterization and is not tested in production.

8.4 Switching Characteristics

over recommended operating free-air temperature range (T_A = +25°C, unless otherwise noted) (1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		TEMP	MIN	TYP	MAX	UNIT
t_{pd}	D	Q	V_{CC}=1.8V±0.15V	C_L=30pF, R_L=1kΩ	FULL	7	21	34	ns
			V_{CC}=2V±0.15V	C_L=30pF, R_L=1kΩ		5.2	15	25	
			V_{CC}=2.5V±0.2V	C_L=30pF, R_L=500Ω		3.5	10	16.5	
			V_{CC}=3.3V±0.3V	C_L=50pF, R_L=500Ω		2.6	8	13	
			V_{CC}=5V±0.5V	C_L=50pF, R_L=500Ω		1.7	7	11.5	
	LE	Q	V_{CC}=1.8V±0.15V	C_L=30pF, R_L=1kΩ	FULL	7.5	23	37	
			V_{CC}=2V±0.15V	C_L=30pF, R_L=1kΩ		6	16	26.5	
			V_{CC}=2.5V±0.2V	C_L=30pF, R_L=500Ω		3.2	10	16.5	
			V_{CC}=3.3V±0.3V	C_L=50pF, R_L=500Ω		2.6	8	13	
			V_{CC}=5V±0.5V	C_L=50pF, R_L=500Ω		1.6	7	11.5	
t_{en}	$\overline{OE}$	Q	V_{CC}=1.8V±0.15V	C_L=30pF, R_L=1kΩ	FULL	6.8	20	32.5	ns
			V_{CC}=2V±0.15V	C_L=30pF, R_L=1kΩ		5	15	25	
			V_{CC}=2.5V±0.2V	C_L=30pF, R_L=500Ω		3	9	15	
			V_{CC}=3.3V±0.3V	C_L=50pF, R_L=500Ω		2.8	7	12	
			V_{CC}=5V±0.5V	C_L=50pF, R_L=500Ω		1.6	6	10	
t_{dis}	$\overline{OE}$	Q	V_{CC}=1.8V±0.15V	C_L=30pF, R_L=1kΩ	FULL	5.8	17	28	ns
			V_{CC}=2V±0.15V	C_L=30pF, R_L=1kΩ		4.5	13	22	
			V_{CC}=2.5V±0.2V	C_L=30pF, R_L=500Ω		3.2	9	15	
			V_{CC}=3.3V±0.3V	C_L=50pF, R_L=500Ω		2.5	7	12	
			V_{CC}=5V±0.5V	C_L=50pF, R_L=500Ω		1.6	6	10	

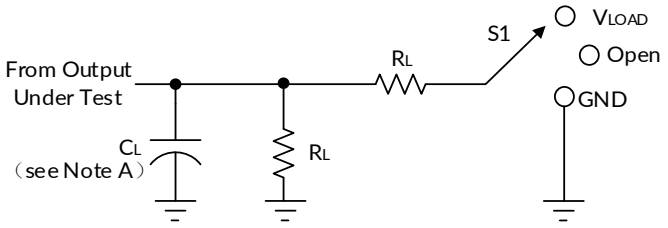
(1) This parameter is ensured by design and/or characterization and is not tested in production.

8.5 Operating Characteristics

T_A = +25°C

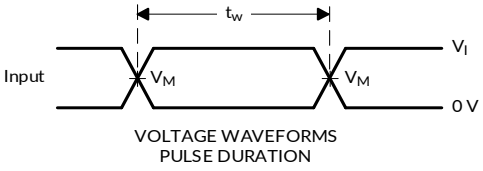
PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd} (Power dissipation capacitance)	Outputs enabled	f = 10 MHz	11	13	16	20	pF
	Outputs disabled		3	3	3	4	

9 PARAMETER MEASUREMENT INFORMATION

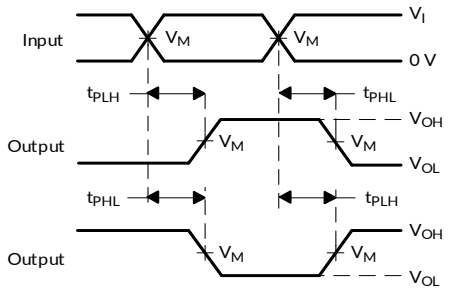


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

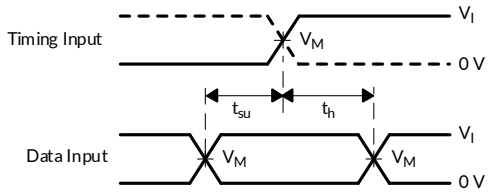
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	1kΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2 x V_{CC}	50pF	500Ω	0.3V



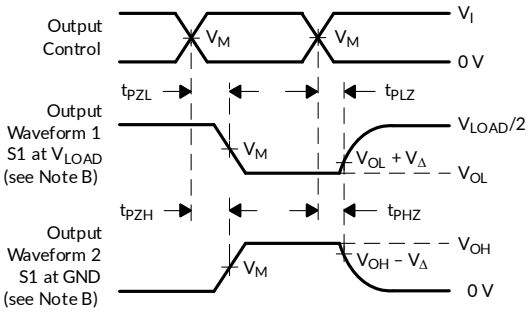
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY
TIMES INVERTION AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES
LOW-AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

10 DETAILED DESCRIPTION

10.1 Overview

A buffered output-enable ($\overline{OE}$) input can be used to place the output in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

10.2 Functional Block Diagram

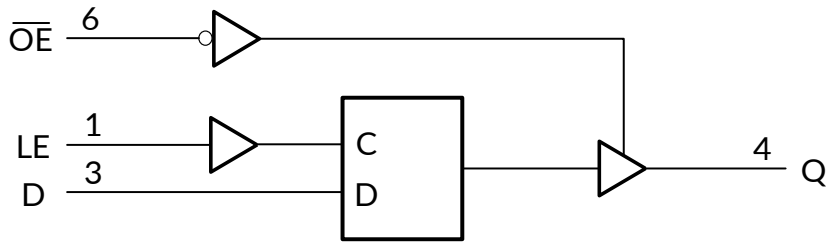


Figure 2. Logic Diagram (Positive Logic)

10.3 Feature Description

10.3.1 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the Electrical Characteristics.

10.3.2 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the Absolute Maximum Ratings.

11 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The RS1G373-Q1 latches can be used to store one bit of data. Figure 3 shows a typical application. The multiplexer is used to convert parallel data coming in from the latch into serial data using the A, B, and C select pins moving up in a sequence. With latch input low by a trigger event, the output Q holds the previous Q0 data entered until the LE pin is cleared.

11.2 Typical Application

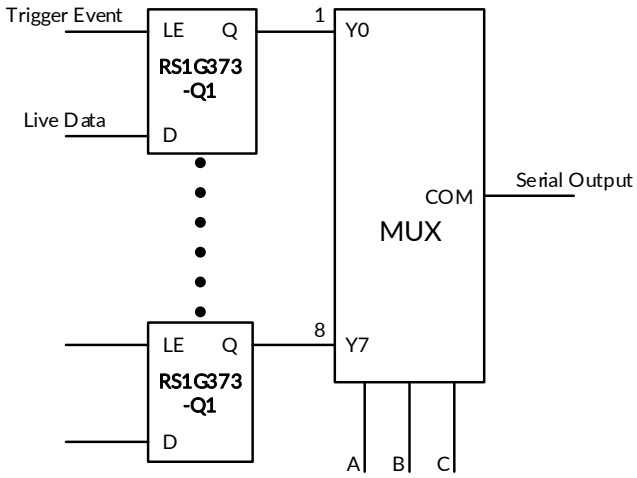


Figure 3. Latch Used with Multiplexer for Parallel to Serial Conversion

11.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

11.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in Recommended Operating Conditions.
   - For specified High and low levels, see V_{IH} and V_{IL} in Recommended Operating Conditions.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions
   - Load currents should not exceed 32 mA per output and 100 mA total through the part.
   - Outputs must not be pulled above V_{CC}.

12 POWER SUPPLY RECOMMENDATIONS

The power supply can be any voltage between the minimum and maximum supply voltage rating located in Recommended Operating Conditions.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, RUNIC recommends a 0.1μF bypass capacitor. If there are multiple V_{CC} pins, RUNIC recommends 0.01μF or 0.022μF bypass capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

13 LAYOUT

13.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 4 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient.

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 5 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

13.2 Layout Example

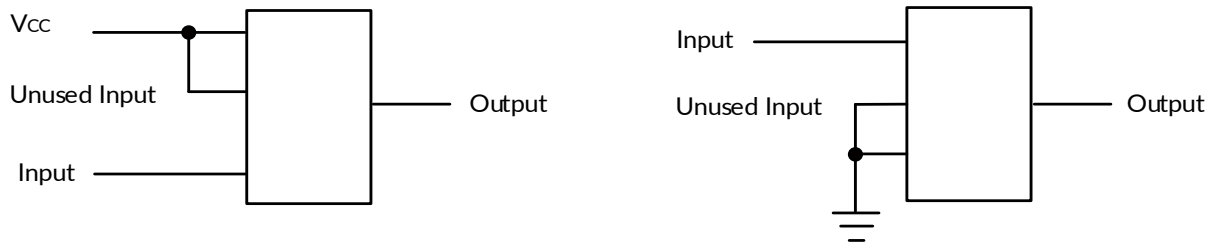


Figure 4. Proper Multiple Input Termination Diagram

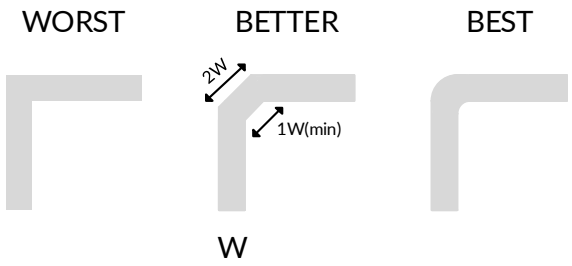
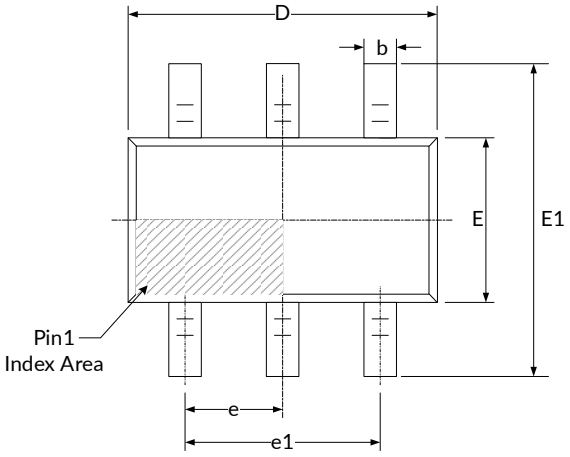
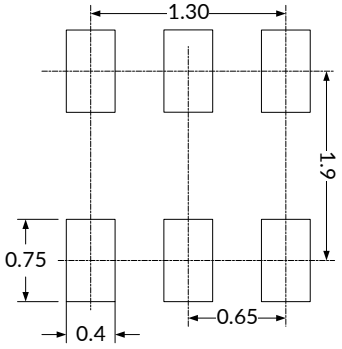


Figure 5. Trace Example

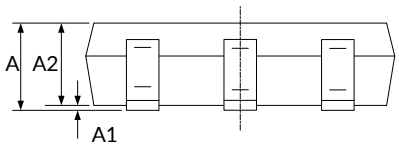
14 PACKAGE OUTLINE DIMENSIONS

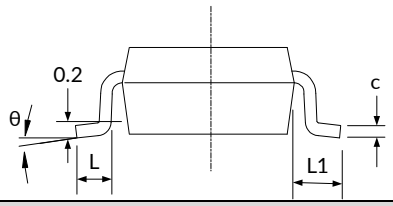
SC70-6 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D (1)	2.000	2.200	0.079	0.087
E (1)	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 (BSC) (2)		0.026 (BSC) (2)	
e1	1.300 (BSC) (2)		0.051 (BSC) (2)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

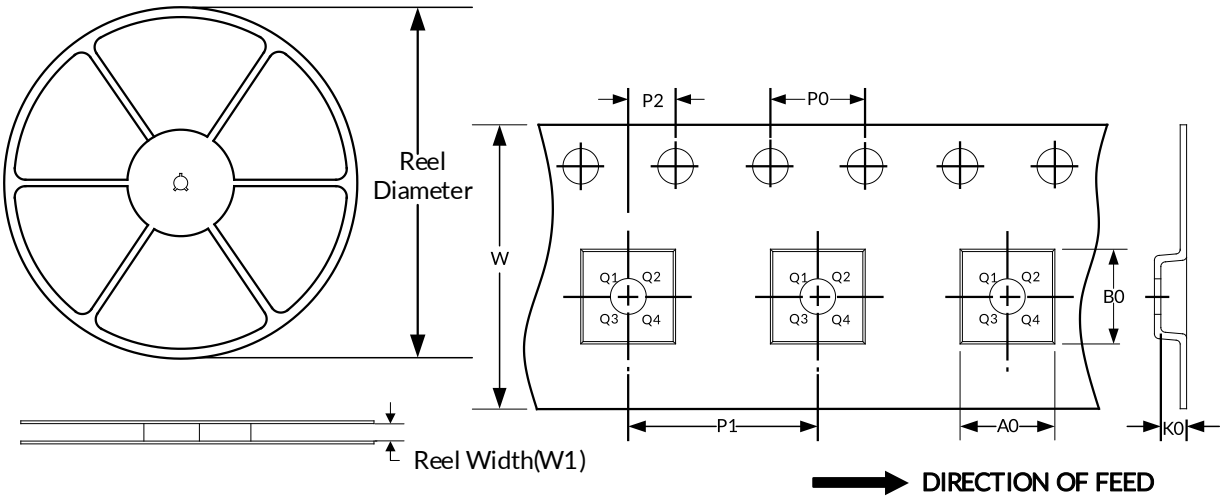
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

15 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SC70-6	7”	9.5	2.40	2.50	1.20	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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